REMARKS/ARGUMENTS

Claims 1 and 2 are pending in this application. By this Amendment, Applicant CANCELS claims 3-5.

Applicant affirms election of Group I and Species II, including claims 1 and 2. Accordingly, claims 3-5 have been canceled since these claims are directed to a non-elected invention. Applicant reserves the right to file a Divisional Application in order to pursue prosecution of non-elected claims 3-5.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mariko (JP 03-276730) in view of Hirano et al. (U.S. 6,849,908). Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishiyama et al. (U.S. 7,087,969) in view of Mariko.

Applicant respectfully traverses the prior art rejections of claims 1 and 2.

Claim 1 recites:

> A semiconductor device, comprising:
> a well of a first conductive type formed in an upper layer of a substrate;
> a low-concentration layer of the first conductive type having a lower impurity concentration than the well, **the low-concentration layer being formed in an extreme surface layer of a channel portion of the well**;
> a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film, the high-k gate dielectric layer being formed on the low-concentration layer;
> a gate electrode formed on the high-k gate dielectric layer; and
> source/drain regions of a second conductive type formed in an upper layer of the well, the source/drain regions sandwiching the low-concentration layer. (emphasis added)

With the unique combination and arrangement of method steps and features recited in Applicant's claim 1, Applicant has been able to provide a semiconductor device that can be controlled with high accuracy by a threshold voltage of the semiconductor device having a high-k gate dielectric layer (see, for example, paragraph [0006] of Applicant's specification).

The Examiner alleged that Mariko teaches "a low-concentration layer 7 of the first conductive p-type having a lower impurity concentration than the well 8, the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8." The Examiner acknowledged that Mariko fails to teach or suggest a gate dielectric layer being a

high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film. The Examiner further alleged that Hirano et al. teaches a high-k gate dielectric layer. Thus, the Examiner concluded that it would have been obvious to one having ordinary skill in the art at the time of the invention to "form a high-k gate dielectric layer/a metal silicate layer served as a gate dielectric film having a higher dielectric constant than a silicon oxide film, as taught by Hirano in the semiconductor device as disclosed by [Mariko] in order to suppress leakage current flowing through the gate dielectric film (see Hirano, col. 6, lines 24-26)." However, Applicant submits that the combination of Mariko and Hirano et al. fails to teach each and every one of the features recited in Applicant's claim 1.

In contrast to the Examiner's allegations, the low concentration p-type surface layer 7 of Mariko is not formed in an extreme surface layer of a channel portion of the high concentration p-type semiconductor region 8, as shown in Figs. 2(a)-2(f) of Mariko. Particularly, Mariko teaches that the portion of the high concentration p-type semiconductor region 8 that the low concentration p-type surface layer 7 is formed on *does not include a channel portion*. The low concentration p-type surface layer 7 is formed on a plateau defined by the top of the high concentration p-type semiconductor region 8. Conversely, as is shown in Applicant's Figs. 2A-2F, a channel including the low-concentration layer is defined on the top of well 3 by the isolation structures 2. Accordingly, Mariko does not teach or suggest the feature of "the low-concentration layer being formed in an extreme surface layer of a channel portion of the well" as is recited in Applicant's claim 1.

Hirano et al. teaches that a metal silicate layer 12a and a gate electrode 24 are formed on a main surface of a silicon substrate 10, as shown in Fig. 4 of Hirano et al. Accordingly, Hirano et al. also fails to teach or suggest the feature of "the low-concentration layer being formed in an extreme surface layer of a channel portion of the well" as is recited in Applicant's claim 1.

Therefore, the Examiner has failed to establish a prima facie case of obviousness of the claimed invention because all the claim features must be taught or suggested by the prior art. See In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974) and MPEP § 706.02(j) and § 2143.03.

Accordingly, Applicant respectfully submits that Mariko and Hirano et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of features recited in claim 1 of the present application.

Claim 2 recites:

> A complementary semiconductor device having a n-type circuit region and a p-type circuit region, comprising:
> a p-type well formed in an upper layer of a substrate of the n-type circuit region;
> a n-type well formed in an upper layer of the substrate of the p-type circuit region;
> **a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well**, the p-type low-concentration layer having a lower impurity concentration than the p-type well;
> **a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well**, the n-type low-concentration having a lower impurity concentration than the n-type well;
> a high-k gate dielectric layer formed on the p-type and n-type low-concentration layers, the high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film;
> a gate electrode formed on the high-k gate dielectric layer;
> n-type source/drain regions formed in an upper layer of the p-type well, the n-type source/drain regions sandwiching the p-type low-concentration layer; and
> p-type source/drain regions formed in an upper layer of the n-type well, the p-type source/drain regions sandwiching the n-type low-concentration layer. (emphasis added)

The Examiner alleged that "Nishiyama discloses in Fig. 1 and related texts as set forth in col. 4, line 45-col. 5, line 30, a complementary semiconductor device having a n-type circuit region 3 and a p-type circuit region 5." The Examiner acknowledged that Nishiyama fails to teach or suggest a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, and a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well. The Examiner further alleged that Mariko teaches "a low-concentration layer 7 of the first conductive p- type having a lower impurity concentration than the well 8, the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8. Thus, the Examiner concluded that it would

have been obvious to one having ordinary skill in the art at the time of the invention "to provide a low-concentration layer formed in an extreme surface layer of a channel portion of the well having a lower impurity concentration than the well … in order to decrease a threshold voltage and to suppress a short-channel effect." However, Applicant submits that the combination of Mariko and Hirano et al. fails to teach each and every one of the features recited in Applicant's claim 2.

As discussed above, the low concentration p-type surface layer 7 of Mariko is not formed in an extreme surface layer of a channel portion of the high concentration p-type semiconductor region 8, as shown in Figs. 2(a)-2(f) of Mariko. Particularly, Mariko teaches that the portion of the high concentration p-type semiconductor region 8 that the low concentration p-type surface layer 7 is formed on *does not include a channel portion*. The low concentration p-type surface layer 7 is formed on a plateau defined by the top of the high concentration p-type semiconductor region 8. Conversely, as is shown in Applicant's Figs. 2A-2F, a channel including the low-concentration layer is defined on the top of well 3 by the isolation structures 2.

Furthermore, Mariko does not teach or suggest an n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well, nor does the Examiner ever provide any explination in the outstanding Office Action about where in the prior art this limitation is taught or suggested. Accordingly, Mariko does not teach or suggest the features of "the low-concentration layer being formed in an extreme surface layer of a channel portion of the well" or "a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well" as is recited in Applicant's claim 2.

Therefore, the Examiner has failed to establish a prima facie case of obviousness of the claimed invention because all the claim features must be taught or suggested by the prior art. See In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974) and MPEP § 706.02(j) and § 2143.03.

Accordingly, Applicant respectfully submits that Nishiyama and Mariko, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of features recited in claim 2 of the present application.

In view of the foregoing remarks, Applicant respectfully submits that claims 1 and 2 are allowable.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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